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OrCAD PLD COMPILER  V4.02   2/7/91  (Source file \ORCAD\MI\LCPTR1.PLD)

  1  This file contains the logic necessary for a GAL16V8 to perform I/O
  2  decoding for the Micro Innovations Low Cost Interface board (LCIF)
  3  depopulated to be the MI Printer Interface board.
  4
  5  Address map:
  6
  7  Printer Data out                   40H
  8  Printer Status in                  40H     (Port 0 dual addressed)
  9  Memory Board Bank Switching Port   42H
 10
 11  I/O Pin Definitions:
 12
 13  |GAL16V8   1:A0,           2:A1,           3:A2,           4:A3,
 14  |          5:A4,           6:A5,           7:A6,           8:A7,
 15  |          9:WR,           11:RD,          12:MEBS,        13:IORQ,
 16  |          14:PTREN,       15:PDATA,       19:PTRSTAT
 17
 18  Acronyms:
 19
 20     Inputs -
 21
 22     A0-A7   = Z80 Address Lines A0 - A7
 23     WR      = Z80 Write Pulse
 24     RD      = Z80 Read Pulse
 25     IORQ    = Z80 I/O Request Pulse
 26
 27     Outputs:
 28
 29     MEBS    = Memory Expansion Board Strobe
 30     PTREN   = Printer Port Enable
 31     PDATA   = Printer Output Data
 32     PTRSTAT = Printer Status Port (Busy & Acknowledge lines)
 33
 34  |  High: A[0..7], PTREN
 35  |
 36  |  PTRSTAT =  IORQ & RD & A7' & A6  & A5' & A4' & A3' & A2' & A1' & A0'
 37  |          &  PTREN
 38  |  PDATA   =  IORQ & WR & A7' & A6  & A5' & A4' & A3' & A2' & A1' & A0'
 39  |          &  PTREN
 40  |  MEBS    =  IORQ & WR & A7' & A6  & A5' & A4' & A3' & A2' & A1  & A0'
 41  |
 42  |
 43  |  Signature: "LCPTR1"
I289  Complex GAL architecture selected.



♀RESOLVED EXPRESSIONS (Reduction 2)

Signal name      Row   Terms

PTRSTAT            1   A0' A1' A2' A3' A4' A5' A6  A7' RD  IORQ  PTREN

PDATA             33   A0' A1' A2' A3' A4' A5' A6  A7' WR  IORQ  PTREN

MEBS              57   A0' A1  A2' A3' A4' A5' A6  A7' WR  IORQ



SIGNAL ASSIGNMENT
                                      Rows
 Pin    Signal name   Column     --------------    Activity
                                 Beg Avail Used

  1.     A0             2        -    -    -        High    (Clock)
  2.     A1             0        -    -    -        High
  3.     A2             4        -    -    -        High
  4.     A3             8        -    -    -        High
  5.     A4            12        -    -    -        High
  6.     A5            16        -    -    -        High
```

7.	A6	20	-	-	-		High	
8.	A7	24	-	-	-		High	
9.	WR	29	-	-	-		Low	
11.	RD	31	-	-	-		Low	(Enable)
12.	MEBS	1	56	8	1		Low	(Three-state)
13.	IORQ	27	48	8	0		Low	(Three-state)
14.	PTREN	22	40	8	0		High	(Three-state)
15.	PDATA	19	32	8	1		Low	(Three-state)
16.	-	14	24	8	0			(Three-state)
17.	-	10	16	8	0			(Three-state)
18.	-	6	8	8	0			(Three-state)
19.	PTRSTAT	1	0	8	1		Low	(Three-state)
				----	----			
				64	3	(5%)		

I200 No fatal errors found in source code.
I201 No warnings.

♀OrCAD PLD
Type: GAL16V8
*
QP20* QF2194* QV1024*
F0*
L0000 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0032 10 10 10 11 10 11 10 11 10 11 01 01 10 10 11 10 *
L1024 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1056 10 10 10 11 10 11 10 11 10 11 01 01 10 10 10 11 *
L1792 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1824 01 10 10 11 10 11 10 11 10 11 01 11 10 10 10 11 *
L2048 01 11 01 10 01 00 11 00 01 00 00 11 01 01 00 00 *
L2080 01 01 01 00 01 01 00 10 00 11 00 01 00 10 00 00 *
L2112 00 10 00 00 11 11 11 11 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 11 *
C20DF*

I202 9/26/91 1:46 pm (Thursday)
I203 Memory utilization 2123/22114 (10%)
I204 Elapsed time 2 seconds

♀